CVM UNIVERSITY
M.Sc. (PHYSICS) Semester-I Examination-2021
Wednesday, 24nd February – 2021
02:00 PM to 04:00 PM
101510102 MICROPROCESSOR & MICROCONTROLLER INTERFACING

Total Marks: 60

Note: (1) Attempt all questions.
(2) Figures to the right indicate marks.

Q. 1 (a) Answer the following multiple choice questions. (08)

(1) Which of the following are known as Higher Address Bus?
a) A15 - A8   b) AD7 - AD0   c) READY   d) WR

(2) MVI A, 20F is an example of?
a) Immediate addressing mode   b) Register addressing mode
c) Direct addressing mode   d) Indirect addressing mode

(3) How are the status of the carry, auxiliary carry and parity flag affected ,if the write instruction
MOV A,#9C
ADD A,#64H
a) CY=0,AC=0,P=0   b) CY=1,AC=1,P=0   c) CY=0,AC=1,P=0
d) CY=1,AC=1,P=1

(4) Which of the following is the default value of stack once after the system undergoes the reset condition? In 8051 microcontroller
a) 08H   b) 09H   c) 00H   d) 07H

(5) All conditional jumps are
a) Absolute jumps   b) Long jumps   c) Short jumps   d) None

(6) The instructions that change the sequence of execution are
a) Conditional instructions   b) Logical instructions
c) Control transfer instructions   d) data transfer instructions

(7) What are the software components in embedded system?
a) Assembler   b) Emulator   c) Compiler   d) All of the above

(8) How many instruction sets are in RISC processor?
a) 16   b) 32   c) 64   d) 128

(b) Answer the following (Fill in the blanks and True or False) (08)

(1) There are _____ general purpose registers in 8085 processor.

(2) Flag register is an 8-bit register having 5 1-bit flip-flops.

(3) _____ & _____ are used for addressing the off-chip data and associated codes respectively by data pointer.

(4) Alternate function of P3.4 is _____

(5) The first byte of a short jump instruction represents op-code byte. (True or False?)

(6) The instruction that is used to complement or invert the bit of a bit addressable SFR is ANL Bit. (True or False?)

(7) A _____ is the heart of the embedded system.

(8) An embedded system has _____ main components which are embedded in it.

Q.2 Attempt any six of the following. (12)

(1) What are the different modes of operation of 8254 programmable timer?
(2) What is data pointer and program counter in 8051 Microcontroller?
(3) Draw the format of the I/O mode and Bit set/reset mode of 8255 PPI.
(4) List out different addressing modes for 8051 microcontroller
(5) Describe all rotate instructions for 8051.
(6) Explain conditional JUMP instructions of 8051.
(7) What is the difference between a simulator and an emulator?
(8) What is the difference between an assembler and a disassembler? State their use in embedded application development.

Q. 3 Draw and Explain the block diagram of 8085 microprocessor and label all the registers. (08)

OR

Q.3 a) Write a program for Convert BCD to Binary number. (08)
b) Six Bytes of Data are stored in memory locations starting at XX50 H. Add all the Data bytes. Use the register to save any carries generated while adding the data bytes. Display the entire sum at the output ports, or store the sum at two consecutive memory locations XX70 H and XX71 H.
DATA (H): A2, FA, DF, E5, 98, 8B. (Using 8085 Microprocessor)

Q. 4 Draw and explain Architecture of 8051 microcontroller. (08)

OR

Q. 4 a) Explain physical difference between Port 0,1,2,3 I/O pins (08)
b) Describe PSW.

Q. 5 a) Write a program to load R7 by data from external RAM location A397 H. (08)
b) Write a program to Multiply the unsigned number in register R3 by the unsigned number on port 2 and put the result in external RAM locations 10H (MSB) and 11H (LSB).

OR

Q. 5 a) Write a program to add 2 integers. Integer 1 is stored at addresses 30H (08) and 31H(low byte at address 30H) , integer 2 is stored at addresses 32H and 33H (low byte at address 32H), the result should be stored at addresses 34H to 36H (low byte at address 34H)
b) Explain Arithmetic and Logical instruction for 8051.

Q. 6 a) Explain role of Integrated Development Environment (IDE) for (08) Embedded software development.
b) Explain Logic Analyser.

OR

Q. 6 a) Write Difference between Von-Neumann & Harvard architectures. (08)
b) Write Difference between CISC and RISC architectures.